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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,955	02/09/2004	Damion T. Searls	884.766US2	4225

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,955	SEARLS ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/04, 2/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 11, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim language "directing a Vcc upwardly" and "retrieving a Vss from the component downwardly" are ambiguous, since Vcc and Vss are voltages and cannot be "directed" or "retrieved".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Mak et al.. As to claim 1, Mak et al., Figure 2, discloses a method of forming a current loop in a decoupling capacitor system, comprising: providing a decoupling capacitor (280)(col. 3, lines 37-38) between an electrical first bump and an electrical second bump (284), wherein the decoupling capacitor includes a Vcc terminal and a Vss terminal; responding to a component transient in connection with the decoupling capacitor, the electrical

first bump and the electrical second bump; directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the component (206), and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump.

As to claims 2, 3 and 4, the simple deflected current loop shown in Figure 2, comprising the electrical connections in lines (286), is within the scope of being a simple current loop, and a simple deflected current loop, since there can be various possible wiring patterns (214),(222),(212) between the capacitor (280) and the component (206).

As to claim 5, Mak et al., Figure 2, discloses that the component transient originates in a component (206), wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the component and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the component, and that terminates in the decoupling capacitor. This current path would pass from the capacitor (280) through the bump (284), the wiring (286), the bump (220), and the wiring (214),(222),(212) to a component (206), then back through the same route to the capacitor.

As to claim 6, Mak et al., Figure 2, discloses that the current loop may be either a simple current loop or a simple deflected current loop.

As to claim 7, Mak et al., Figure 2, discloses that the component transient originates in a component disposed in a top structure (205), wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the top structure and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the top structure, and that terminates in the decoupling capacitor.

As to claim 8, Mak et al., Figure 2, discloses that the current loop may be either a simple current loop or a simple deflected current loop.

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by applicants prior art. As to claim 1, applicants prior art, Figure 11, discloses a method of forming a current loop in a decoupling

capacitor system, comprising: providing a decoupling capacitor (30) between an electrical first bump, to the immediate left of the capacitor, and an electrical second bump, immediately to the right of the capacitor, wherein the decoupling capacitor includes a Vcc terminal and a Vss terminal; responding to a component transient in connection with the decoupling capacitor, the electrical first bump and the electrical second bump; directing a Vcc upwardly from the decoupling capacitor (66) and the electrical first bump toward the component, and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump. The current path from the component downward through the second bump, to the immediate right of the capacitor, and ending at the Vss side of the capacitor may be formed exactly as the current path (72), since the set of solder bumps are indistinguishable from each other.

As to claims 2, 3 and 4, the simple deflected current loop shown in Figure 11 is within the scope of being a simple current loop, and a simple deflected current loop.

As to claim 5, applicants prior art discloses (Spec. page 1) that the component transient originates in a component (26), wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the component and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the component, and that terminates in the decoupling capacitor.

As to claim 6, applicants prior art, Figure 11, discloses that the current loop is a simple deflected current loop.

As to claim 7, applicants prior art, Figure 11, and the specification, page 1, discloses that the component transient originates in a component disposed in a top structure (24), wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the top structure and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the top structure, and that terminates in the decoupling capacitor.

As to claim 8, applicants prior art, Figure 11, discloses that the current loop is a simple deflected current loop.

As to claim 9, applicants prior art, Figure 11, discloses that the component transient originates in an interposer, formed under component (26), disposed in a top structure (24), wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the interposer and retrieving a Vss from the interposer downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the interposer, and that terminates in the decoupling capacitor.

As to claim 10, applicants prior art, Figure 11, discloses that the component transient originates in a socket, which may also be the structure formed under component (26), disposed in a top structure, wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the socket and retrieving a Vss from the interposer downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the socket, and that terminates in the decoupling capacitor.

Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Mak et al.. Mak et al., Figure 2, discloses a method of forming a current loop in a decoupling capacitor, the system including a component (206), comprising: providing a decoupling capacitor (280) between an electrical first bump and an electrical second bump (284) wherein the decoupling capacitor includes a Vcc terminal and a Vss terminal; responding to a component transient in connection with the decoupling capacitor, the electrical first bump and the electrical second bump; directing a Vcc upwardly from the decoupling capacitor (284) and the electrical first bump toward the component (206); and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the component and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the component, and that terminates in the decoupling capacitor, and wherein the current loop is a simple deflected current loop.

Claims 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by applicants prior art. As to claim 11, applicants prior art, Figure 11, discloses a method of forming a current loop in a decoupling capacitor, the system including a component (26), comprising: providing a decoupling capacitor (30) between an electrical first bump, to the immediate left of the capacitor, and an electrical second bump, to the immediate right of the capacitor, wherein the decoupling capacitor includes a Vcc terminal and a Vss terminal; responding to a component transient in conpection with the decoupling capacitor, the electrical first bump and the electrical second bump; directing a Vcc upwardly from the decoupling capacitor (66) and the electrical first bump toward the component (26); and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, wherein directing a Vcc upwardly from the decoupling capacitor and the electrical first bump toward the component and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the decoupling capacitor, that passes through the component, and that tenninates in the decoupling capacitor, and wherein the current loop is a simple deflected current loop. The current path from the component downward through the second bump, to the immediate right of the capacitor, and ending at the Vss side of the capacitor may be formed exactly as the current path (72), since the set of solder bumps are indistinguishable from each other.

As to claims 12 and 13, applicants prior art, Figure 11, discloses that the component (26) is formed on a structure, which, taken together with the component forms top structure (24). It is understood in the art that this structure may be a socket or interposer, consistent with established means of mounting semiconductor components.

Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Mak et al.. Mak et al., Figure 2, discloses a method of forming a current loop in a system, the system including: a substrate (250) including a substrate first pad and a substrate second pad (282); an electrical first bump (284) including a bottom end and a top end, wherein the bottom end is adhered to the first pad; an electrical second bump including a bottom end and a top end, wherein the bottom end is adhered to the second pad; a first decoupling capacitor (280) disposed above the substrate and substantially contiguous to the electrical first bump; and a top structure (205) disposed at the electrical first bump top end, wherein the top

structure is in electrical communication with the first decoupling capacitor the method including: responding to a transient in the electrical component in connection with the first decoupling capacitor, the electrical first bump and the electrical second bump; directing a Vcc upwardly from the first decoupling capacitor and the electrical first bump toward the component; and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, wherein directing a Vcc upwardly from first decoupling capacitor and the electrical first bump toward the component and retrieving a Vss from the component downwardly toward the first decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the first decoupling capacitor, that passes through the component, and that terminates in the first decoupling capacitor, and wherein the current loop is a simple deflected current loop.

Claims 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by applicants prior art. As to claim 14, applicants prior art, Figure 11, discloses a method of forming a current loop in a system, the system including: a substrate (12) including a substrate first pad, to the immediate left of the capacitor, and a substrate second pad, to the immediate right of the capacitor; an electrical first bump including a bottom end and a top end, wherein the bottom end is adhered to the first pad; an electrical second bump including a bottom end and a top end, wherein the bottom end is adhered to the second pad; a first decoupling capacitor (30) disposed above the substrate and substantially contiguous to the electrical first bump; and a top structure (24) disposed at the electrical first bump top end, wherein the top structure is in electrical communication with the first decoupling capacitor the method including: responding to a transient in the electrical component in connection with the first decoupling capacitor, the electrical first bump and the electrical second bump; directing a Vcc upwardly from the first decoupling capacitor and the electrical first bump toward the component; and retrieving a Vss from the component downwardly toward the decoupling capacitor and the electrical second bump, wherein directing a Vcc upwardly from first decoupling capacitor and the electrical first bump toward the component and retrieving a Vss from the component downwardly toward the first decoupling capacitor and the electrical second bump, includes forming a current loop that originates in the first decoupling capacitor, that passes through the component, and that terminates in the first decoupling capacitor, and wherein the current loop is a simple

deflected current loop. The current path from the component downward through the second bump, to the immediate right of the capacitor, and ending at the Vss side of the capacitor may be formed exactly as the current path (72), since the set of solder bumps are indistinguishable from each other.

As to claims 15 and 16, applicants prior art, Figure 11, discloses that the component (26) is formed on a structure, which, taken together with the component forms top structure (24). It is understood in the art that this structure may be a socket or interposer, consistent with established means of mounting semiconductor components.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
February 13, 2006